EXHIBIT 6

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group:	2822
Confirmation No.:	4085
Application No.:	11/338,007
Invention:	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE
Applicant:	James A. Cooper et al.
Filed:	January 23, 2006
Attorney Docket:	3220-79132
Examiner:	Patton, Paul E.

Certificate Under 37 CFR 1.8(a)

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, fax number (571) 273-8300

on August 6, 2007

(Signature)

Glen M. Kellett
(Printed Name)

AMENDMENT AND REPLY

MAIL STOP AMENDMENT
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated April 4, 2007, please consider the following:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of the claims in this application:

1. (Currently Amended) A metal-oxide semiconductor field-effect transistor comprising:

a ~~semiconductor~~ silicone-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a first source region;

a second source region; and

a JFET region formed on a front side of the current spreading semiconductor layer and defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities.

2. (Cancelled)

3. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the JFET region has a width of less than about three micrometers.

4. (Original) The metal-oxide semiconductor field-effect transistor of claim 3, wherein the JFET region has a width of about one micrometer.

5. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the third concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

6. (Cancelled)

7. (Currently Amended) The metal-oxide semiconductor field-effect transistor of claim ~~6~~ 1, wherein the current spreading semiconductor layer has a fourth concentration of first type impurities that is greater than the second concentration of first type impurities.

8. (Original) The metal-oxide semiconductor field-effect transistor of claim 7, wherein the fourth concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

9. (Currently Amended) The metal-oxide semiconductor field-effect transistor of claim ~~6~~ 8, wherein the JFET region has a width of about one micrometer.

10. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

11. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

12. (Currently Amended) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a ~~semiconductor~~ silicone-carbide substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a first source region;

a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other;

a second source region; ~~and~~

a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

13. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a width of about one micrometer.

14. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

15-16. (Cancelled)

17. (Currently Amended) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a semiconductor substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

~~a first source region;~~

~~a second source region; and~~

a plurality of first and second source regions;

a plurality of base contact regions; and

a JFET region defined between the plurality of first source ~~region~~ regions and the plurality of second source ~~region~~ regions, the JFET region being formed on a front side of the current spreading semiconductor layer,

wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

18. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the current spreading semiconductor layer has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

19. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 18, wherein the first concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

20. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the JFET region has a width of about three micrometers or less.

21-22. (Cancelled)

23. (Original) A vertical double-implanted metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer epitaxially formed on a front side of the silicon-carbide substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer epitaxially formed on a front side of the drift layer, the current spreading semiconductor layer having a third concentration of first type impurities greater than the second concentration of first type impurities;

a first source region;

a second source region; and

a JFET region defined between the first source region and the second source region and formed on a front side of the current spreading semiconductor layer, the JFET region having a width less than about three micrometers and a fourth concentration of first type impurities greater than the second concentration of first type impurities.

REMARKS

The Office Action dated April 4, 2007 has been carefully reviewed. Claims 1-23 stand rejected in the 4/4/2007 Office Action. Additionally, the declaration filed on May 18, 2006 is found defective in the 4/4/2007 Office Action. By this amendment, claims 2, 6, 15, 16, 21, and 22 are cancelled without prejudice. Claims 1, 7, 9, 12, and 17 are amended.

DECLARATION

The Examiner found the declaration filed on May 18, 2006 to be defective because the signature of the second named inventor, Ms. Asmita Saha, was lacking. Applicants file herewith a new declaration signed by the second named inventor, Ms. Asmita Saha. A copy of the originally filed declaration, which is signed by the first named inventor, Mr. James A. Cooper, is also included for the convenience of the Office.

SECTION 102(e) REJECTION OF INDEPENDENT CLAIM 1

The Examiner rejected independent claim 1 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication No. 2003/0227052 A1 to Ono et al. (hereinafter "Ono"). This claim has been amended to include the subject matter of dependent claims 2 and 6. Claims 2 and 6 have been cancelled. Regarding claim 2, the Examiner rejected this claim under 35 U.S.C. §103(a) as being unpatentable over Ono in view of U.S. Patent No. 6,573,534 B1 to Kumar et al. (hereinafter "Kumar"). Regarding claim 6, the Examiner rejected this claim under 35 U.S.C. §103(a) as being unpatentable over Ono in view of U.S. Patent No. 6,137,139 to Zeng et al. (hereinafter "Zeng").

The Combination of Ono, Kumar, and/or Zeng fails to Render Amended Claim 1 Obvious

Claim 1 has been amended to recite "a silicone-carbide substrate having a first concentration of first type impurities" and "a current spreading semiconductor layer formed on a front side of the drift semiconductor layer." In forming the rejection of claim 1, the Examiner bases his rejection on Ono, but concedes that "Ono does not disclose that the semiconductor substrate is a silicon-carbide substrate." The Examiner relies on Kumar to overcome this deficiency of Ono. The Examiner asserts:

> Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar (Column 1, lines 27-30). 4/4/2007 Office Action, Paragraph 11, Page 5.

Applicants strongly disagree. As noted by the Examiner, Ono and Zeng are directed toward MOSFET devices having silicon substrates, while Kumar is directed toward silicon-carbide MOSFET devices. Although the Examiner asserts that modifying Ono to include a silicon-carbide is an obvious modification, such an assertion ignores the technical aspects of silicon-carbide MOSFET devices. Silicon-carbide MOSFET devices are often used for high-power applications. In such applications, a high blocking voltage is desirable. For example, Kumar teaches:

> It is an object of the present invention to provide a SiC MOS transistor which makes full use of the characteristics of SiC in order to obtain even lower ON resistance and *higher breakdown voltage* than conventional SiC MOS transistors. Kumar, Col 1, ll. 31-35, emphasis added.

Unlike silicon MOSFET devices, the blocking voltage of silicon-carbide MOSFET devices is limited by gate oxide failure rather than semiconductor breakdown. Gate oxide failure can be caused by the magnetic field of the gate oxide having an excessive strength. As noted in Paragraph [0028] of Applicants' present patent application, the use of a JFET region and/or a current spreading layer in a silicon-carbide substrate reduces the blocking voltage of the

device due to an increased strength of the gate oxide magnetic field. As such, it would not be obvious to one of ordinary skill in the art to use the features of Ono or Zeng with a silicon-carbide substrate because such features would reduce the blocking voltage of the device and likely render the device inoperable for its intended purpose (i.e., high power applications). Thus, it is clear that no one of ordinary skill in the art would combine Ono or Zeng with Kumar in the manner proposed by the Examiner. As such, amended claim 1 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 3-4 and 7-11

Claims 3-4 and 7-11 include claim 1 as a base claim. As such, the rejection of claims 3-4 and 7-11 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 1. In light of the reasons for withdrawal of the rejection of claim 1, any arguments specific to claims 3-4 and 7-11 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution. Claims 7 and 9 have been amended for consistency.

SECTION 102(e) REJECTION OF INDEPENDENT CLAIM 12

The Examiner rejected independent claim 12 under 35 U.S.C. §102(e) as being anticipated by Ono. Claim 12 has been amended to recite:

> 12. A double-implanted metal-oxide semiconductor field-effect transistor comprising:
> a silicone-carbide substrate;
> a drift semiconductor layer formed on a front side of the semiconductor substrate;
> a first source region;
> a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other;
> a second source region;
> a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other; and

> a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

Anticipation exists only if all the elements of the claimed invention are present in a product or process disclosed, expressly or inherently, in a single prior art reference. *Hazeltine Corp. v. RCA Corp.*, 468 U.S. 1228 (1984). Ono fails to disclose or teach each and every element of amended claim 12. Accordingly, amended claim 12 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 13 and 14

Claims 13 and 14 include claim 12 as a base claim. As such, the rejection of claims 13 and 14 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 12. In light of the reasons for withdrawal of the rejection of claim 12, any arguments specific to claims 13 and 14 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

SECTION 103(a) REJECTION OF INDEPENDENT CLAIM 17

The Examiner rejected claim 17 under 35 U.S.C. §103(a) as being unpatentable over Ono in view of Zeng. Claim 17 has been amended to include the subject matter of claim 22. In regard to claim 22, the Examiner rejected this claim under 35 U.S.C. §103(a) as being unpatentable over Ono in view of Zeng and further in view of U.S. Patent Publication Serial No. 2003/0052329 to Kobayashi et al. (hereinafter "Kobayashi"). In support of this rejection, the Examiner asserts that:

> Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of base contact regions (13), form alternating strips of N-type doped regions and P-type doped regions, *the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.* 4/4/2007 Office Action, Paragraph 37, Page 10, emphasis added.

Applicants disagree. First, reference numeral 13 of Kobayashi points to a well region (13) and reference numeral 17 of Kobayashi points to a gate insulation film (17). Applicants assume the Examiner meant to refer to the contact region 21 and the source region 15 of Kobayashi, respectively. Regardless, Kobayashi simply fails to teach such a configuration. Rather, it is clear from a review of FIGS. 17 and 18 of Kobayashi that the source electrode 19 (see FIG. 17) is oriented in a **parallel configuration** (i.e., non-orthogonal) relative to the source region 15 and the contact region 21. Therefore, for at least this reason, the combination of Ono, Zeng, and Kobayashi fails to render amended claim 17 obvious. As such, claim 17 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 18-20

Claims 18-20 include claim 17 as a base claim. As such, the rejection of claims 18-20 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 17. In light of the reasons for withdrawal of the rejection of claim 17, any arguments specific to claims 18-20 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

SECTION 103(a) REJECTION OF INDEPENDENT CLAIM 23

The Examiner rejected claim 32 under 35 U.S.C. §103(a) as being unpatentable over Ono in view of Zeng in further view of Tokura and in further view of Kumar. In forming this rejection, the Examiner concedes that "Ono does not disclose that the semiconductor substrate is silicon-carbide." The Examiner again relies on Kumar to overcome this deficiency of Ono. The Examiner asserts:

> Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using a silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance according to the teachings of Kumar. 4/4/2007 Office Action, Page 13-14, Paragraph 50.

However, for all of the reasons provided above in regard to independent claim 1, it would not be obvious to one of ordinary skill to modify the teaching of Ono in the manner suggested by the Examiner. For at last this reason, the combination of Ono, Zeng, Tokura, and Kumar fails to render claim 23 obvious. As such, claim 23 is believed to be in condition for allowance and such action is respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that this application is in a condition for allowance. Action to that end is hereby solicited. If there are any questions or comments that would speed prosecution of this application, the Examiner is invited to call the undersigned at (317) 261-7959.

It is respectfully requested that this paper be considered as a petition for a two-month extension of time extending the deadline of this response to August 4, 2007. The Commissioner is hereby authorized to charge the fee of $450.00 for this two-month extension of time, and any shortages or overpayments of fees, to the Account of Barnes & Thornburg, Deposit Account No. 10-0435 with reference to file 3220-79132.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group:	2822
Confirmation No.:	4085
Application No.:	11/338,007
Invention:	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE
Applicant:	James A. Cooper et al.
Filed:	January 23, 2006
Attorney Docket:	3220-79132
Examiner:	Patton, Paul E.

ELECTRONICALLY SUBMITTED ON: MARCH 12, 2008

RESPONSE TO ACCOMPANY REQUEST FOR CONTINUED EXAMINATION

MAIL STOP RCE
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated October 12, 2007, and contemporaneously with the filing of a Request for Continued Examination, Applicants submit the following:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of the claims in this application:

1. (Currently Amended) A metal-oxide semiconductor field-effect transistor comprising:

a ~~silicone carbide~~ silicon-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a first source region;

a second source region; and

a JFET region formed on a front side of the current spreading semiconductor layer and defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities.

2. (Cancelled)

3. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the JFET region has a width of less than about three micrometers.

4. (Original) The metal-oxide semiconductor field-effect transistor of claim 3, wherein the JFET region has a width of about one micrometer.

5. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the third concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

6. (Cancelled)

7. (Previously Presented) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the current spreading semiconductor layer has a fourth concentration of first type impurities that is greater than the second concentration of first type impurities.

8. (Original) The metal-oxide semiconductor field-effect transistor of claim 7, wherein the fourth concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

9. (Previously Presented) The metal-oxide semiconductor field-effect transistor of claim 8, wherein the JFET region has a width of about one micrometer.

10. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

11. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

12. (Currently Amended) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a ~~silicone carbide~~ silicon-carbide substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a first source region;

a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;

a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;

a second source region;

a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;

a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

13. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a width of about one micrometer.

14. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

15-16. (Cancelled)

17. (Currently Amended) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a semiconductor substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a plurality of first and second source regions;

a plurality of base contact regions; and

a JFET region defined between the plurality of first source regions and the plurality of second source regions, the JFET region being formed on a front side of the current spreading semiconductor layer,

wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, each of the alternating strips defining a longitudinal axis that is ~~being~~ substantially orthogonal to a longitudinal axis defined by respective source electrodes formed over the first and the second source regions.

18. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the current spreading semiconductor layer has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

19. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 18, wherein the first concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

20. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the JFET region has a width of about three micrometers or less.

21-22. (Cancelled)

23. (Original) A vertical double-implanted metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer epitaxially formed on a front side of the silicon-carbide substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer epitaxially formed on a front side of the drift layer, the current spreading semiconductor layer having a third concentration of first type impurities greater than the second concentration of first type impurities;

a first source region;

a second source region; and

a JFET region defined between the first source region and the second source region and formed on a front side of the current spreading semiconductor layer, the JFET region having a width less than about three micrometers and a fourth concentration of first type impurities greater than the second concentration of first type impurities.

REMARKS

The Office Action dated October 12, 2007 has been carefully reviewed. Claims 1, 3-5, 7-14, 17-20, and 23 are pending in this application. Claims 1, 3-5, 7-14, 17-20, and 23 stand rejected in the 10/12/2007 Office Action. By this amendment, claims 1, 12, and 17 are amended.

35 U.S.C. §103(a) REJECTIONS

The Examiner rejected claims 1, 3, 4, 7-10, 12, and 13 as being unpatentable over Ono (U.S. Patent Publication No. 2003/0227052 A1) in view of Kumar (U.S. Patent No. 6,573,534 B1) in further view of Zeng (U.S. Patent No. 6,137,139). The Examiner rejected claims 11 and 17-29 as being unpatentable over Ono in view of Kumar in further view of Zeng and in further view of Kobayashi (U.S. Patent Publication Serial No. 2003/0052329). The Examiner rejected claims 5, 14, and 23 as being unpatentable over Ono in view of Kumar in further view of Zeng and in further view of Tokura (U.S. Patent No. 5,545,908).

Discussion: Independent Claim 1 - Ono, Kumar, & Zeng

In support of the rejection of claim 1, the Examiner concedes that "Ono does not disclose that the semiconductor substrate is a silicon-carbide substrate." (10/12/2007 Office Action, page 3, paragraph 4). The Examiner relies on Kumar to overcome this deficiency of Ono and states that Kumar "discloses that the substrate is a silicon-carbide substrate." (10/12/2007 Office Action, page 3, paragraph 5). The Examiner also concedes that "Ono as modified by Kumar does not explicitly disclose that a current spreading layer is formed on a front side of the drift semiconductor layers; and where the concentration of impurities of the first type is greater that [sic] the concentration of impurities of the first type in the drift region by at least one order of magnitude." (10/12/2007 Office Action, page 4, paragraph 9). The Examiner relies on Zeng to over this deficiency of Ono and Kumar. In an attempt to establish a reason to combine the teachings of Ono, Kumar, and Zeng, the Examiner argues that:

> [I]t would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono by using as silicon-carbide substrate for advantages such as higher breakdown voltage and lower ON resistance

> according to the teachings of Kumar (Column 1, lines 27-30). . . .
>
> [i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ono to have a current spreading layer formed on a front side of the drift semiconductor layer; and wherein the concentration of impurities of the first type is greater that [sic] the concentration of impurities of the first type in the drift region by at least one order of magnitude for advantages such as reduced on-resistance without degrading device ruggedness and reliability according to the teachings of Zeng (Column 4, lines 32039). (10/12/2007 Office Action, page 4, paragraph 7 and page 5, paragraph 12)

Applicants respectfully traverse these rejections. As discussed in detail below, Applicants believe that no rational reason exists why one of ordinary skill in the art would combine Ono, Kumar, and Zeng in the manner described. Applicants assert that no such reason exists because the proposed combination would render the device of Ono unsatisfactory or inoperable for its intended purpose. Thus, Ono, Kumar, and Zeng teach away from the proposed combination and cannot support a finding of obviousness.

I. References Teach Away from Proposed Combination

Applicants assert that no rational reason exists to combine Ono, Kumar, and Zeng in the manner described by the Examiner because the cited references teach away from the proposed combination. The Supreme Court recently emphasized the "principle that when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious." KSR Int'l v. Teleflex, Inc., 127 S.Ct. 1727, 1740 (citing U.S. v. Adams, 383 U.S. 39, 51-52 (1966). According to the Federal Circuit, the prior art effectively teaches away when an examiner's proposed modification of prior art renders the prior art invention "inoperable for its intended purpose." In re Gordon, 733 F.2d 900, 902 (Fed. Cir. 1984). "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." (see MPEP §2141.01.V)

The semiconductor device of Ono would be render unsatisfactory or inoperable for its intended purpose if modified to include the structures of Zeng and Kumar as proposed by

the Examiner. As noted by the Examiner, Ono and Zeng are directed toward MOSFET devices having silicon substrates, while Kumar is directed toward silicon-carbide MOSFET devices. Although the Examiner asserts that modifying Ono to include a silicon-carbide is an obvious modification, such an assertion ignores the technical aspects of silicon-carbide MOSFET devices. Silicon-carbide MOSFET devices are often used for high-power applications. In such applications, a high blocking voltage is desirable. For example, Kumar teaches:

> It is an object of the present invention to provide a SiC MOS transistor which makes full use of the characteristics of SiC in order to obtain even lower ON resistance and *higher breakdown voltage* than conventional SiC MOS transistors. Kumar, Col 1, ll. 31-35, emphasis added.

Unlike silicon MOSFET devices, the blocking voltage of silicon-carbide MOSFET devices is limited by gate oxide failure rather than semiconductor breakdown. Gate oxide failure can be caused by the electric field of the gate oxide having an excessive strength. As noted in Paragraph [0028] of Applicants' present patent application, the use of a JFET region and a current spreading layer in a silicon-carbide substrate reduces the blocking voltage of the device due to an increased strength of the gate oxide electric field. As such, it would not be obvious to one of ordinary skill in the art to incorporate a JFET region as taught in Ono and a current spreading layer as taught in Zeng with a silicon-carbide substrate because such features would reduce the blocking voltage of the device and likely render the device inoperable for its intended purpose. For example, such modification to the power MOSFET 1 of Ono would render the device unsatisfactory or inoperable for its intended purpose as a power device due to a reduced blocking voltage. Applicants, however, have discovered various methods and structures, such as increasing the thickness of the drift layer, wherein a JFET region and a current spreading layer may be incorporated in a silicon-carbide substrate while maintaining a high blocking voltage (see, e.g., Paragraph [0028] of Applicants' present patent application).

For at least the reasons provided above, there simply is no motivation combine Ono, Kumar, and Zeng in the manner proposed by the Examiner because such a modification would render the resultant device unsatisfactory in operation. As such, amended claim 1 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 3-4 and 7-11

Claims 3-4 and 7-11 include claim 1 as a base claim. As such, the rejection of claims 3-4 and 7-11 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 1. In light of the reasons for withdrawal of the rejection of claim 1, any arguments specific to claims 3-4 and 7-11 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

Discussion: Independent Claim 12 - Ono, Kumar, & Zeng

The Examiner appears to reject claim 12 as being unpatentable over the combination of Ono, Kumar, and Zeng. For the reasons provided below, the rejection of claim 12 is traversed.

I. Examiner Has Failed to Provide Explanation Of Rejection

The Examiner has failed to provide an explicit rejection of claim 12. Applicants respectfully request that the Examiner point with particularity to those sections of Ono, Kumar, and/or Zeng wherein the Examiner believes each element of claim 12 is disclosed as required by 37 C.F.R. §1.104(c)(2):

> In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

II. Combination Fails To Disclose Each Element Of Claim 12

Applicants believe that no reference of record discloses each and every element of amended claim 12. Claim 12 has been amended to further clearly define the claimed invention. In particular, claim 12 has been amended to recite:

> 12. A double-implanted metal-oxide semiconductor field-effect transistor comprising:
> a silicon-carbide substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;
a first source region;
a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;
a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;
a second source region;
a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;
a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and
a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

None of the references of record individually or in combination disclose such a device. For example, neither Ono, Kumar, nor Zeng disclose the particular configuration of base contact regions and source regions as claimed.

III. References Teach Away from Proposed Combination

The Examiner rejected claim 12 as unpatentable over the combination of Ono, Kumar, and Zeng. As such, all the arguments provided above in regard to claim 1 apply with equal force to claim 12. Accordingly, for at least the reasons provided herein, amended claim 12 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 13 and 14

Claims 13 and 14 include claim 12 as a base claim. As such, the rejection of claims 13 and 14 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 12. In light of the reasons for withdrawal of the rejection of claim 12, any arguments specific to claims 13 and 14 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

Discussion: Independent Claim 17 - Ono, Kumar, Zeng, & Kobayashi

The Examiner maintains his rejection of claim 17 based on the combination of Ono, Kumar, Zeng, and Kobayshi. In support of this rejection, the Examiner asserts that:

> Kobayashi shows (Fig 18) a plurality of source regions and a plurality of base contact regions, wherein the plurality of base contact regions (13), form alternating strips of N-type doped regions and P-type doped regions, *the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions.* (10/12/2007 Office Action, Page 8, Paragraph 20, emphasis added).

The Examiner later expounds upon this rejection:

> As to claim 17, this claim is rejected on the same basis as before. While it is true that Kobayashi has a drawing with limited detail, [t]he format claimed of the individual devices laid out in strips is very well known in the art of power transistors. Further, the source contacts would inherently be laid out orthogonal from the strip direction as can be also inferred from figure 12 of Tokura. (10/12/2007 Office Action, Page 12, Paragraph 33).

Applicants disagree. First, Kobayashi fails to disclose the particular structure relied on by the Examiner. Second, the Examiner appears to be taking improper Official Notice regarding the configuration of power transistors. Third, the Examiner improperly argues that the claimed configuration is inherent in the cited reference. Thus, for at least these reasons, the Examiner's rejection of claim 17 is improper and should be withdrawn.

I. Kobayshi Fails To Disclose The Structure Relied On By Examiner

Again, Applicants point out that reference numeral 13 of Kobayashi points to a well region (13) and reference numeral 17 of Kobayashi points to a gate insulation film (17). Applicants assume the Examiner meant to refer to the contact region 21 and the source region 15 of Kobayashi, respectively. Regardless, Kobayashi simply fails to teach "a plurality of source regions and a plurality of base contact regions, wherein the plurality of base contact regions (13), form alternating strips of N-type doped regions and P-type doped regions, the alternating strips (17) being substantially orthogonal to respective source electrodes formed over the first and second source regions" as asserted by the Examiner. Rather, it is clear from a review of FIGS.

17 and 18 of Kobayashi that the source electrode 19 (see FIG. 17) is oriented in a **parallel configuration** (i.e., non-orthogonal) relative to the source region 15 and the contact region 21.

However, to further clearly define the invention of claim 17, Applicants have amended claim 17 to recite:

> wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, each of the alternating strips defining a longitudinal axis that is substantially orthogonal to a longitudinal axis defined by respective source electrodes formed over the first and the second source regions

Neither Kobayashi nor any other reference of record teaches such a structure. If the Examiner upholds his rejection of claim 17 based on Kobayashi, Applicants respectfully request the Examiner point with particularly to the figure(s) and associated description of Kobayashi wherein such an element is disclosed.

II. Official Notice is Improper

The Examiner appears to take official notice that "[t]he format claimed of the individual devices laid out in strips is very well known in the art of power transistors." However, such official notice is improper because such a configuration is clearly not well known and the Examiner has failed to provide a technical line of reasoning supporting the official notice (see MPEP §2144.03.A and §2144.03.B). Applicants specifically challenge such an official notice because the claimed configuration of "wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, each of the alternating strips defining a longitudinal axis that is substantially orthogonal to a longitudinal axis defined by respective source electrodes formed over the first and the second source regions" is not common knowledge, being rather an invention of the Applicants.

II. Claimed Configuration Is Not Inherent

The Examiner argues that "the source contacts would inherently be laid out orthogonal from the strip direction as can be also inferred from figure 12 of Tokura." "Inherency, however, may not be established by probabilities or possibilities. The mere fact that

a certain thing may result from a given set of circumstances is not sufficient." *Hansgirg v. Kemmer*, 102 F.2d 212, 40 U.S.P.Q. 665, 667 (C.C.P.A. 1939); *In re Oelrich and Divigard*, 666 F.2d 578, 212 U.S.P.Q. 323, 326 C.C.P.A. 1981). Accordingly, it cannot be said that the source contacts of Kobayashi must be orthogonal to the strip direction of the base and source regions. Applicants note that Figure 12 of Tokura is of no help either. As such, the device configuraiton of claim 17 is neither inherent nor obvious in light of the teachings of Kobayashi, Tokura, nor any other reference of record. For at least the reasons provdied above, amended claim 17 is believed to be in condition for allowance and such action is respectfully requested.

Discussion Re: Claims 18-20

Claims 18-20 include claim 17 as a base claim. As such, the rejection of claims 18-20 should be withdrawn for the reasons hereinbefore discussed with regard to amended claim 17. In light of the reasons for withdrawal of the rejection of claim 17, any arguments specific to claims 18-20 are held in abeyance without prejudice or admission to any assertion made by the Examiner in order to expedite prosecution.

Discussion: Independent Claim 23 - Ono, Kumar, Zeng, & Tokura

The Examiner rejected claim 23 as unpatentable over the combination of Ono, Kumar, Zeng, and Tokura. As such, for all the reasons provided above in regard to independent claim 1, it would not be obvious to one of ordinary skill to combine the teachings of Ono, Kumar, and Zeng in the manner proposed by the Examiner. For at last this reason, the combination of Ono, Zeng, Tokura, and Kumar fails to render claim 23 obvious. As such, claim 23 is believed to be in condition for allowance and such action is respectfully requested.

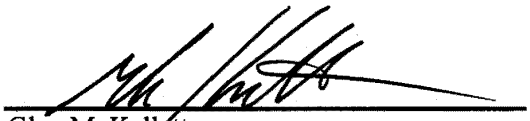
CONCLUSION

In view of the foregoing, it is submitted that this application is in a condition for allowance. Action to that end is hereby solicited. If there are any questions or comments that would speed prosecution of this application, the Examiner is invited to call the undersigned at (317) 261-7959.

It is respectfully requested that this paper be considered as a petition for a two-month extension of time extending the deadline of this response to March 12, 2008. The Commissioner is hereby authorized to charge the fee of $460.00 for this two-month extension of time, and any shortages or overpayments of fees, to the Account of Barnes & Thornburg, Deposit Account No. 10-0435 with reference to file 3220-79132.

Respectfully submitted,

BARNES & THORNBURG LLP



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group:	2822	
Confirmation No.:	4085	
Application No.:	11/338,007	
Invention:	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE	**DATED:** **AUGUST 22, 2008**
Applicant:	James A. Cooper et al.	
Filed:	January 23, 2006	
Attorney Docket:	3220-79132	
Examiner:	Patton, Paul E.	

RESPONSE TO OFFICE ACTION

MAIL STOP AF
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated June 25, 2008, Applicants submit the following:

Amendments to the Claims, which begin on page 2 of this pager; and

Remarks, which begin on page 7 of this paper.

CLAIMS AS PENDING

1. (Currently Amended) A metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a first source region;

a second source region; ~~and~~

a JFET region formed on a front side of the current spreading semiconductor layer and defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities;

a plurality of source regions; and

a plurality of base contact regions,

wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

2. (Cancelled)

3. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the JFET region has a width of less than about three micrometers.

4. (Original) The metal-oxide semiconductor field-effect transistor of claim 3, wherein the JFET region has a width of about one micrometer.

5. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the third concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

6. (Cancelled)

7. (Previously Presented) The metal-oxide semiconductor field-effect transistor of claim 1, wherein the current spreading semiconductor layer has a fourth concentration of first type impurities that is greater than the second concentration of first type impurities.

8. (Original) The metal-oxide semiconductor field-effect transistor of claim 7, wherein the fourth concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

9. (Previously Presented) The metal-oxide semiconductor field-effect transistor of claim 8, wherein the JFET region has a width of about one micrometer.

10. (Original) The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

11. (Cancelled)

12. (Previously Presented) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a first source region;

a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;

a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;

a second source region;

a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;

a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

13. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a width of about one micrometer.

14. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

15-16. (Cancelled)

17. (Previously Presented) A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a semiconductor substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a plurality of first and second source regions;

a plurality of base contact regions; and

a JFET region defined between the plurality of first source regions and the plurality of second source regions, the JFET region being formed on a front side of the current spreading semiconductor layer,

wherein the plurality of first and second source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, each of the alternating strips defining a longitudinal axis that is substantially orthogonal to a longitudinal axis defined by respective source electrodes formed over the first and the second source regions.

18. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the current spreading semiconductor layer has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

19. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 18, wherein the first concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

20. (Original) The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the JFET region has a width of about three micrometers or less.

21-23. (Cancelled)

REMARKS

Applicants thank the Examiner for consideration of the present application. This response is filed in response to the Office Action, dated June 25, 2008, to place this application in condition for allowance as suggested by the Examiner. In the 06/25/08 Final Office Action, the Examiner rejected claims 1, 3-5, and 7-10. The Examiner objected to claim 11, but indicated that this claim would be allowable if rewritten to include all the limitations of the base claim. Applicants note with appreciation the Examiner's indication that claims 12-14 and claims 17-20 are in condition for allowance. By this amendment, claim 1 is amended and claims 11 and 23 are cancelled.

DISCUSSION: Independent Claim 1

Claim 1 has been amended to include each element of claim 11. As such, claim 1 is believed to be in condition for allowance and such action is respectfully requested. In addition, claims 1, 3-5, and 7-10 each include claim 1 as a base claim. Accordingly, each of claims 1, 3-5, 7-10 is also believed to be in condition for allowance and such action is respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that this application is in a condition for allowance. Action to that end is hereby solicited. If there are any questions or comments that would speed prosecution of this application, the Examiner is invited to call the undersigned at (317) 261-7959.

It is respectfully requested that, if necessary to effect a timely response, this paper be considered as a Petition for an Extension of Time sufficient to effect a timely response. The

Commissioner is hereby authorized to charge the fee for such Petition and any shortage of fees, and credit any overpayment of fees, to the Account of Barnes & Thornburg, Deposit Account No. 10-0435 with reference to file 3220-79132.

Respectfully submitted,

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/Glen Kellett/

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INDS02 GKELLETT 985239v1

Notice of Allowability	Application No. 11/338,007	Applicant(s) COOPER ET AL.	
	Examiner PAUL E. PATTON	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed August 22, 2008.*.

2. ☒ The allowed claim(s) is/are *1,3-5,7-10,12-14 and 17-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Response to Amendment

1. Acknowledgement is made of Amendment filed August 22, 2008.

Allowable Subject Matter

2. Claims 1, 3-5, 7-10, 12-14 and 17-20 are allowed.

3. The following is an examiner's statement of reasons for allowance: The prior art of record taken alone or in combination fails to anticipate or render obvious a plurality of source regions and a plurality of base contact regions forming alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions along with all the other limitations as recited in independent claims 1 and 17; or a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis; a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode; a second source region; a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis; a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart fro each other in a direction parallel to the longitudinal axis defined by the second source electrode, along with all the other limitations of claim 12..

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL E. PATTON whose telephone number is (571)272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/
Supervisory Patent Examiner, Art Unit 2822

Paul E Patton
Examiner
Art Unit 2822

/P. E. P./
Examiner, Art Unit 2822